Standardization Imperatives for Chiplets on Autonomous Drive

François Piednoël
Distinguished mSoC Standard Chief Architect
Mercedes-Benz Research & Development North America, Inc.

Mercedes-Benz
Das Beste oder nichts.

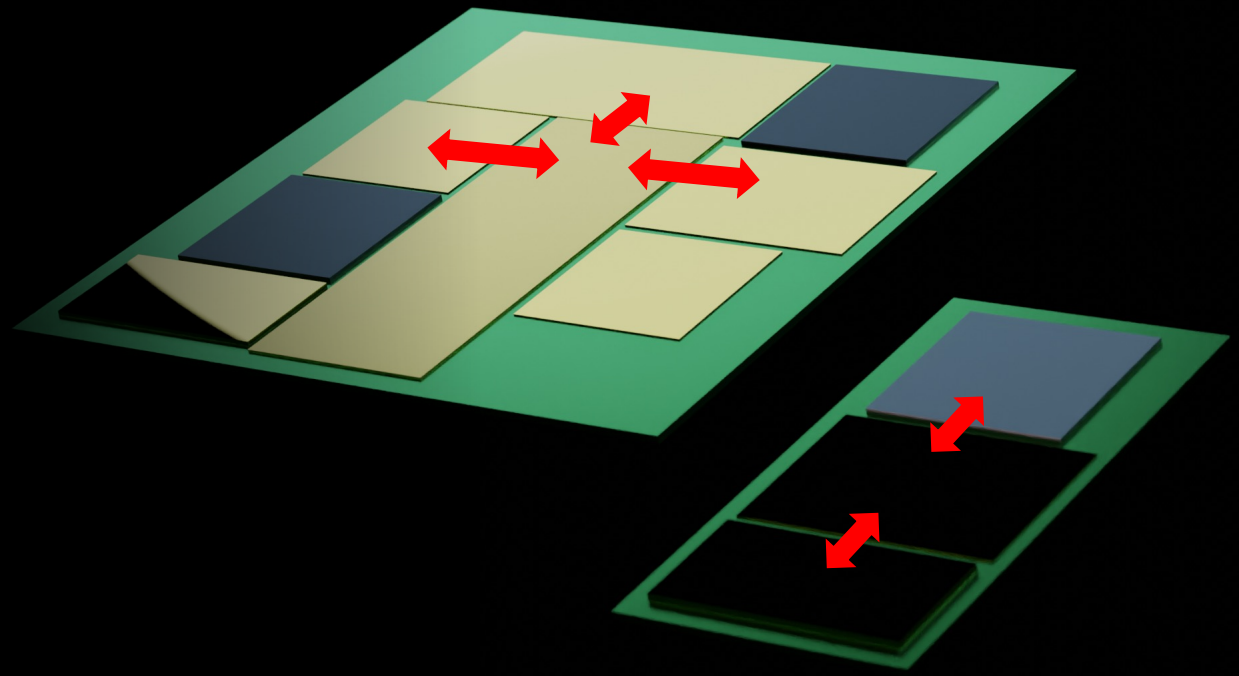
About me …

20 years at Intel, Bluetooth in 1997…
Creation of the Pentium IV extreme Edition
Performance Lead Architect for 11 years, Conroe to Skylake
Lead of SKULLTRAIL Platform

4.3 Years at Mercedes-Benz:
Working on making Level 4 Autonomy a reality
UCIe™ Consortium Member

The Interconnects standard

Join UCIe™ consortium.



- Same chiplet can go into different form factors
- Creating/Improve Time to market.

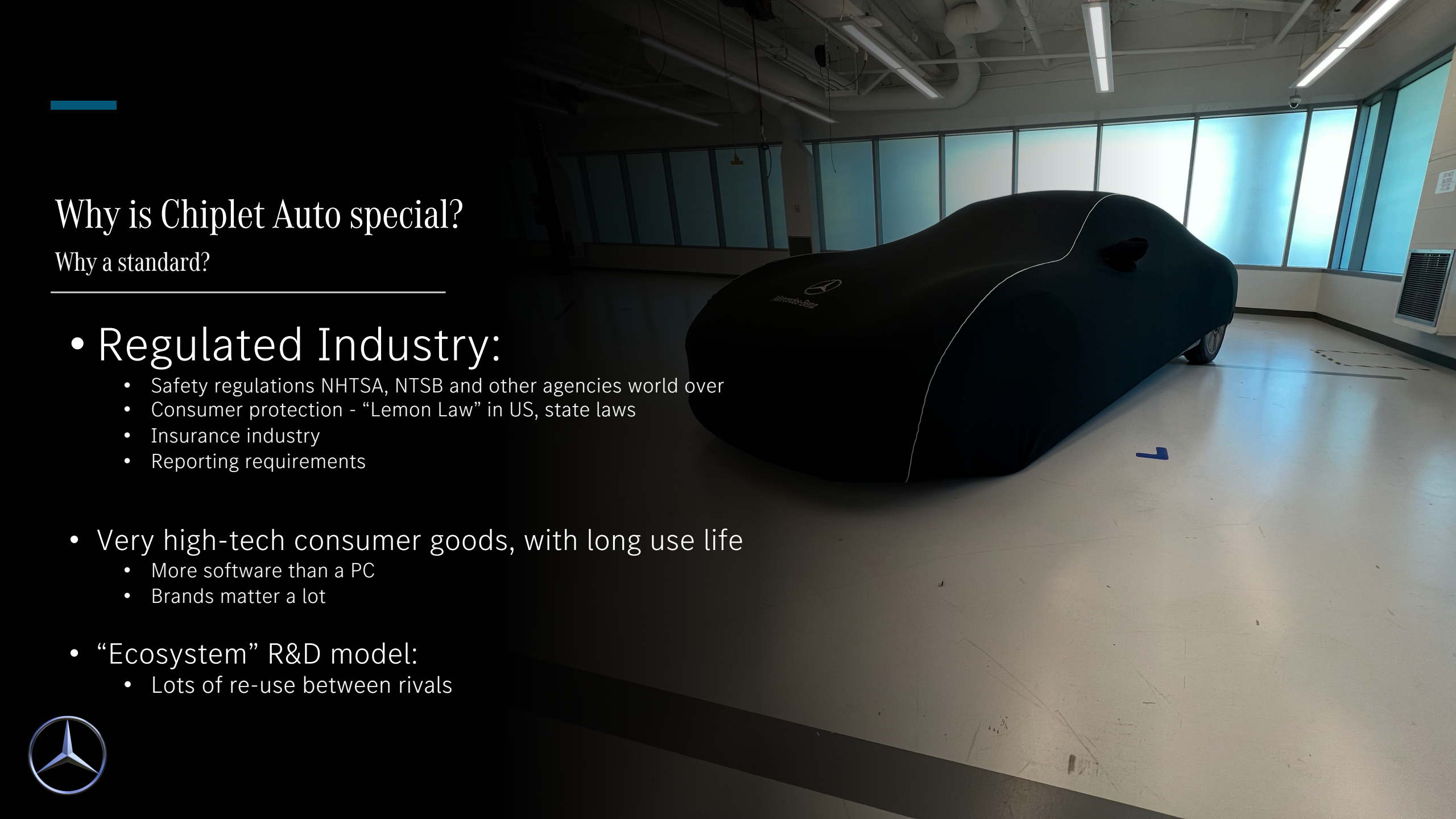
Why is Chiplet Auto special?

Why a standard?

- Regulated Industry:
  - Safety regulations NHTSA, NTSB and other agencies world over
  - Consumer protection - “Lemon Law” in US, state laws
  - Insurance industry
  - Reporting requirements

- Very high-tech consumer goods, with long use life
  - More software than a PC
  - Brands matter a lot

- “Ecosystem” R&D model:
  - Lots of re-use between rivals

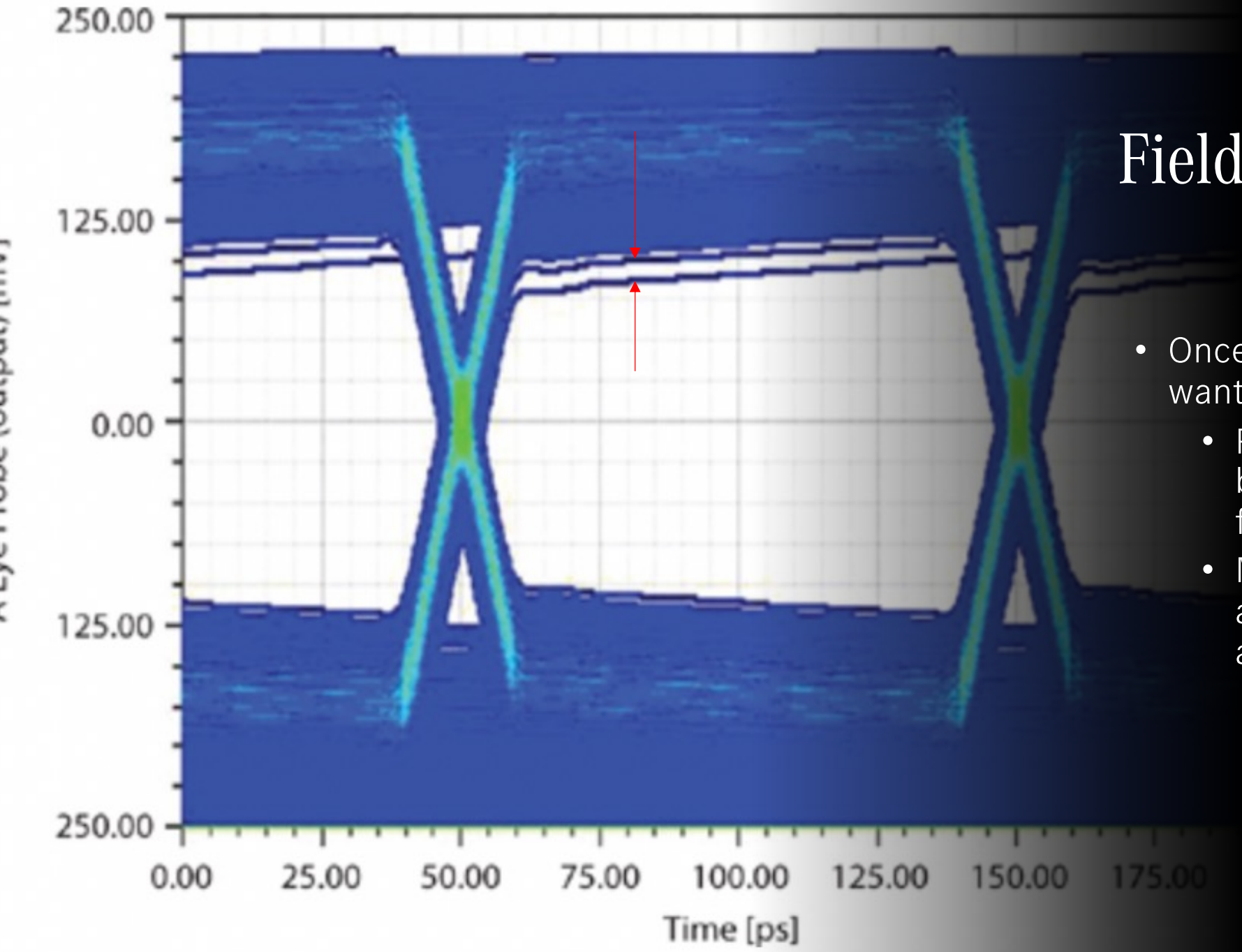


Goals of Chiplet for Auto Standardization

- Safety:
  - Avoid injury
  - Avoid damage
- Fault tolerance and serviceability/repairability:
  - Financial burden of warranty
  - Brand image risk
- Ecosystem and costs:
  - Share and Re-use as much as possible, Optimized licensing

Preventive Monitoring

- Need to be able to monitor the link health over life
  - Life of vehicle/computer
  - Life of the Fleet
  - Several times per day
- Detect potential failures:
  - Idiosyncratic – per computer random failures due to aging
  - Physical – e.g., thermal cycling related micro-bump failures
  - Pattern dependent – some marginality in specific design makes “lane number X fail every time a computer fails”
- Close to actual use conditions:
  - Mission mode capture of key parameters
  - Timestamp along with data from other sensors (temperature, voltage etc.) for offline diagnostics



Field Repairability

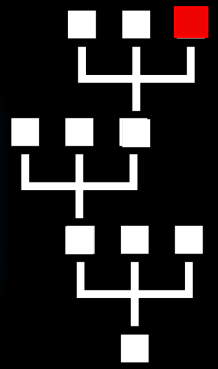
- Once potential problem detected – want to fix it:
  - Redundancy already exists; can be invoked on re-training and/or forced by software
  - Micro-bump Failure rates under auto conditions with large advanced packages can be high

Mission:

Mercedes-Benz: Home of only certified Level 3 and Level 4 Parking

Functional safety
Causes
Increases in
processing power

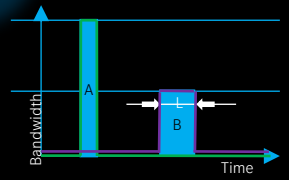
Performance
Sensitivity
Architecture



Level 2/3/4 Power Efficient

Gigabytes
Per
Seconds

Latency
Sensitivity



Hardware and Software Standardization

SAFE | EFFICIENT | FAST

UEFI & UCIe

Performance Needs of Level 4 Data From the Prototype:

Machine learning + Physic laws Checks

The computing size : GIGA Scale on CPU

Peak Instructions 48,600,000,000

About 48 cores of IPC = 1.0 (instruction per clock)

Optimize code ~1.8 IPC ➔ 1.8 x 48 = 86 Cores

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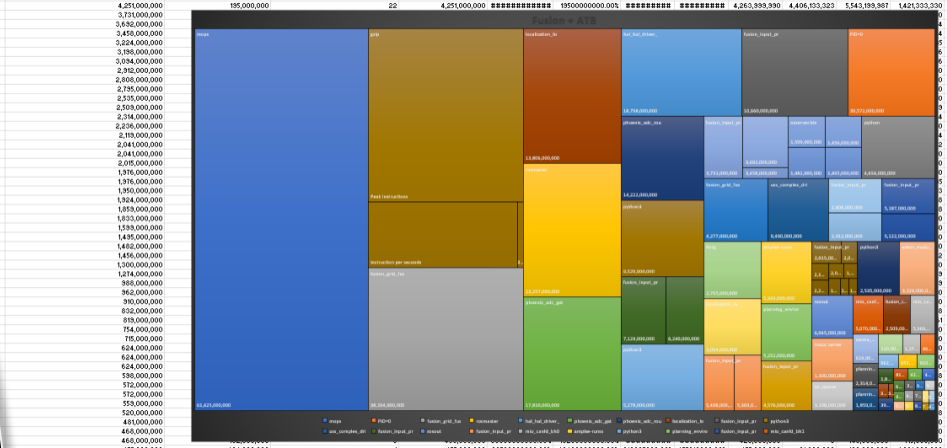
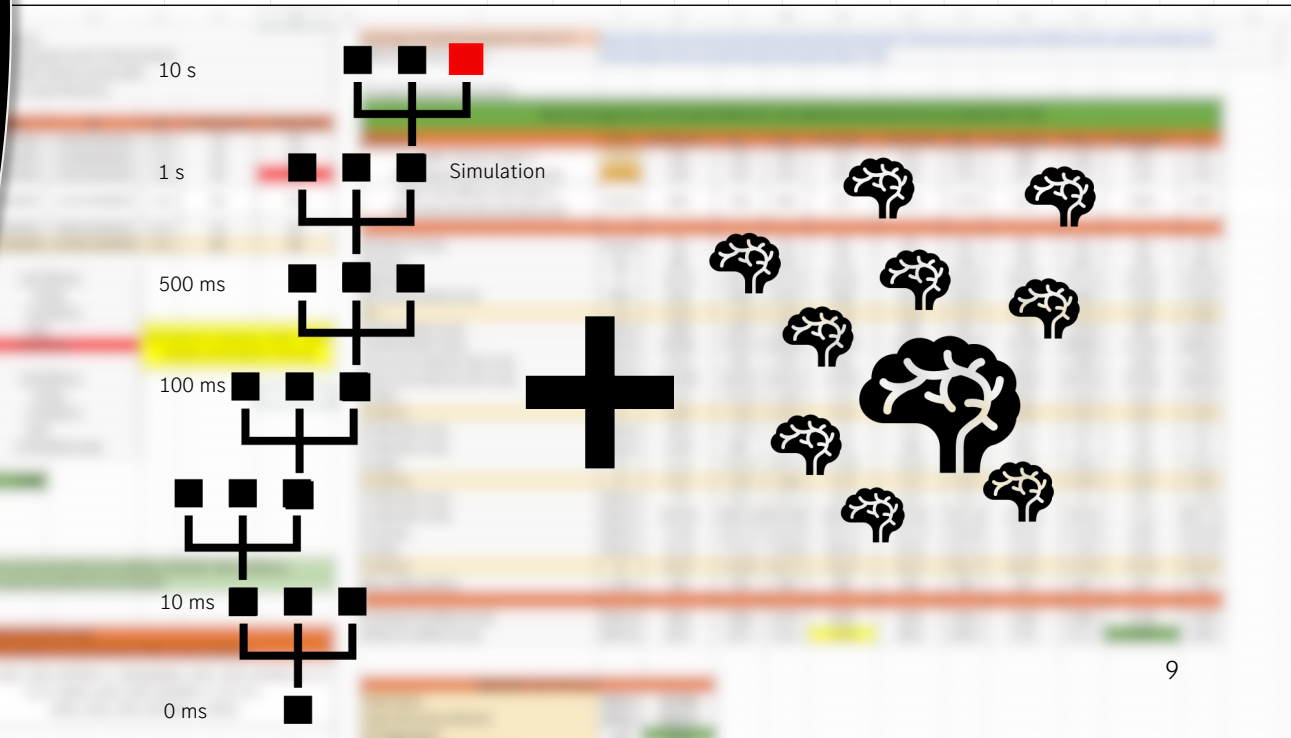
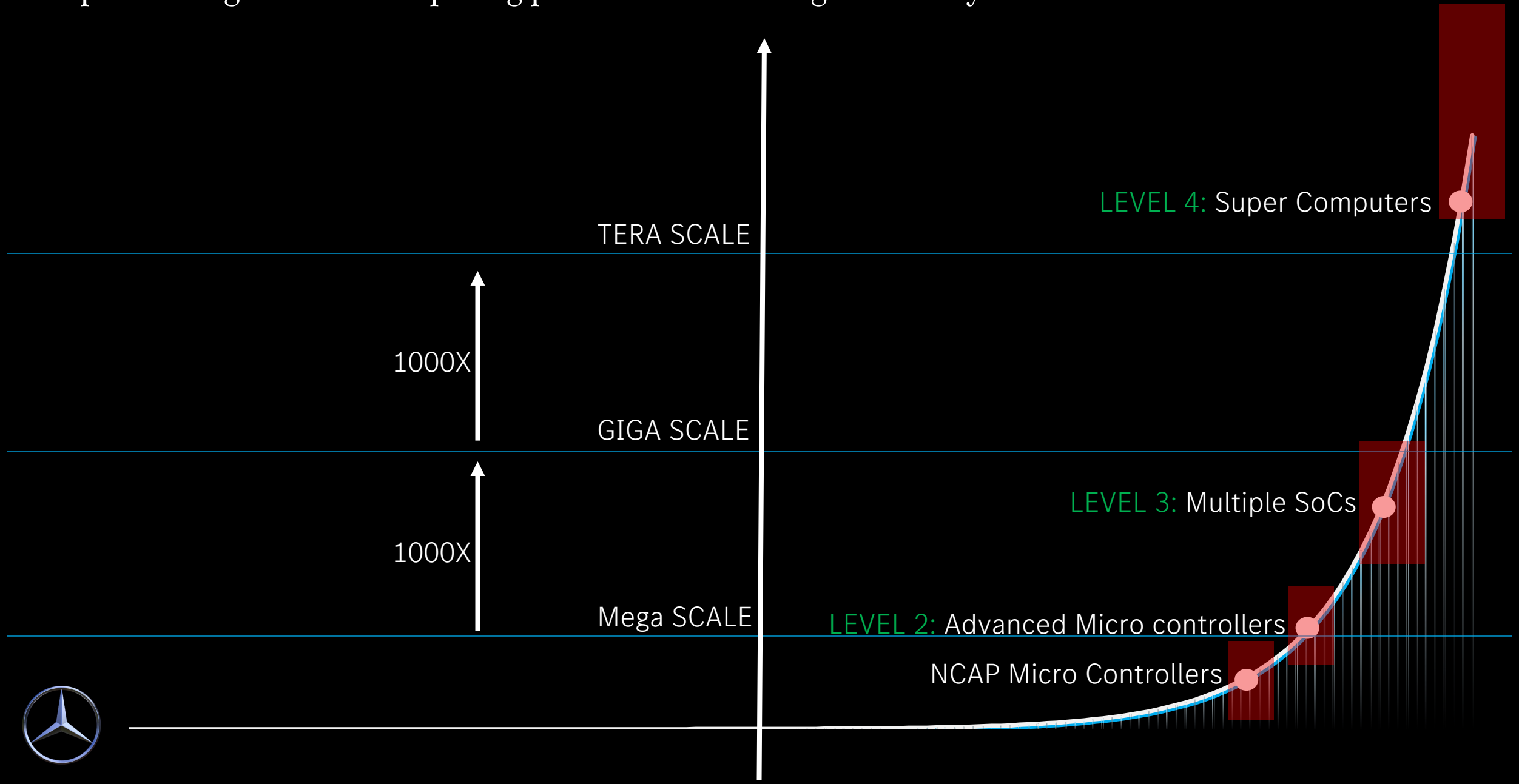
TERA Scale on Machine Learning

TERA Scale on Memory Bandwidth

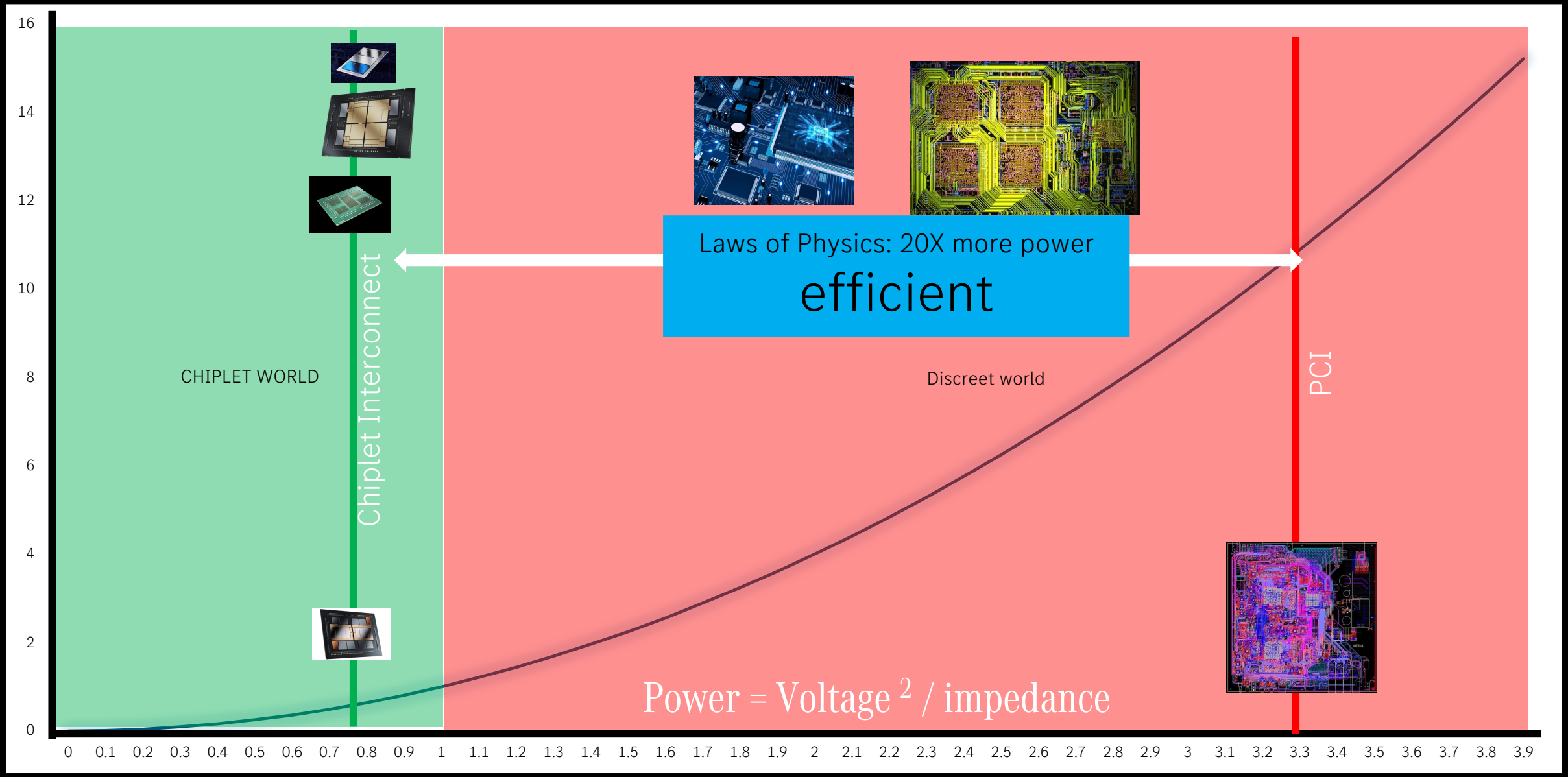




Exponential growth of computing power for increasing Autonomy

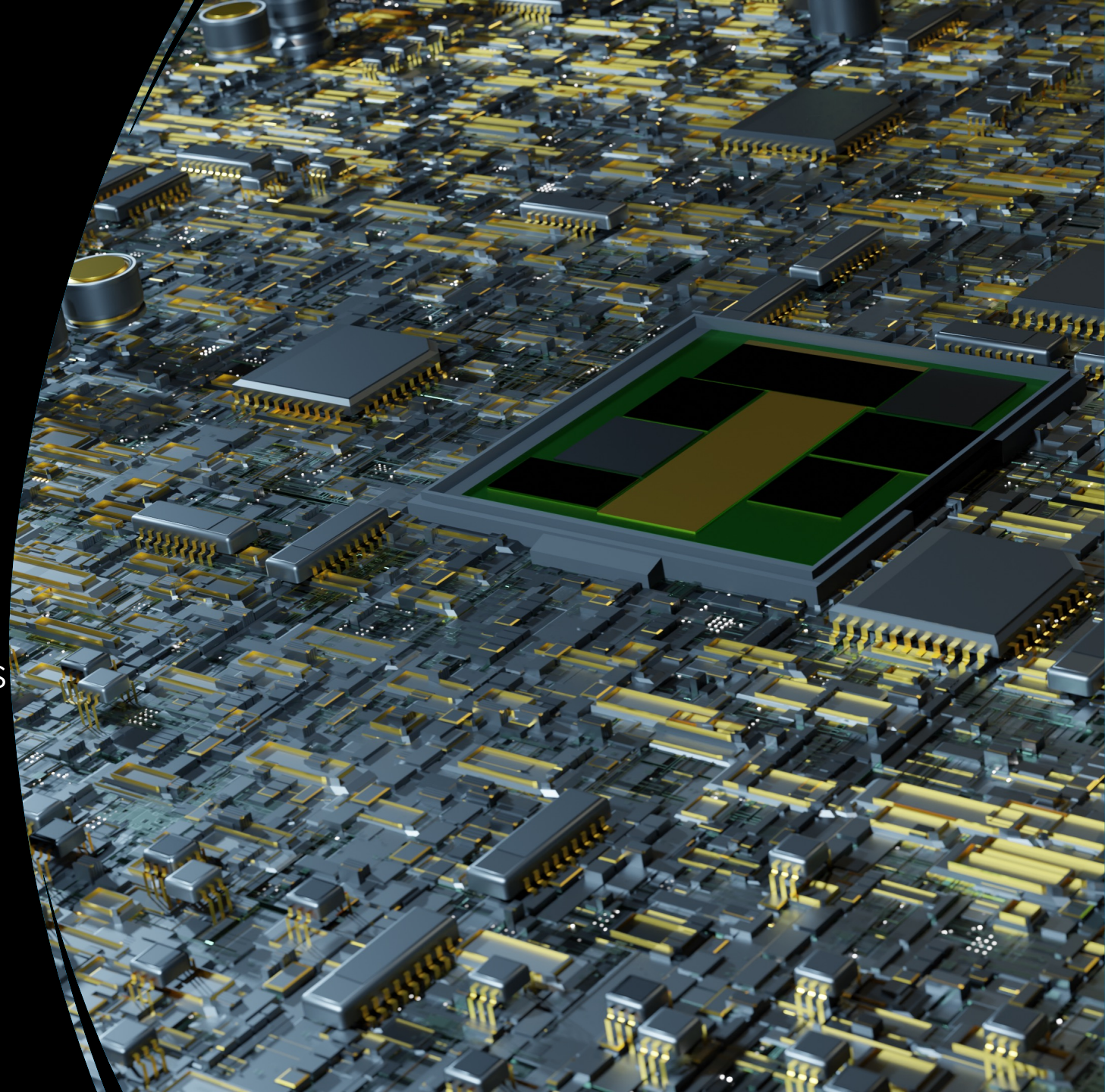


Power = Voltage ^{2} / impedance



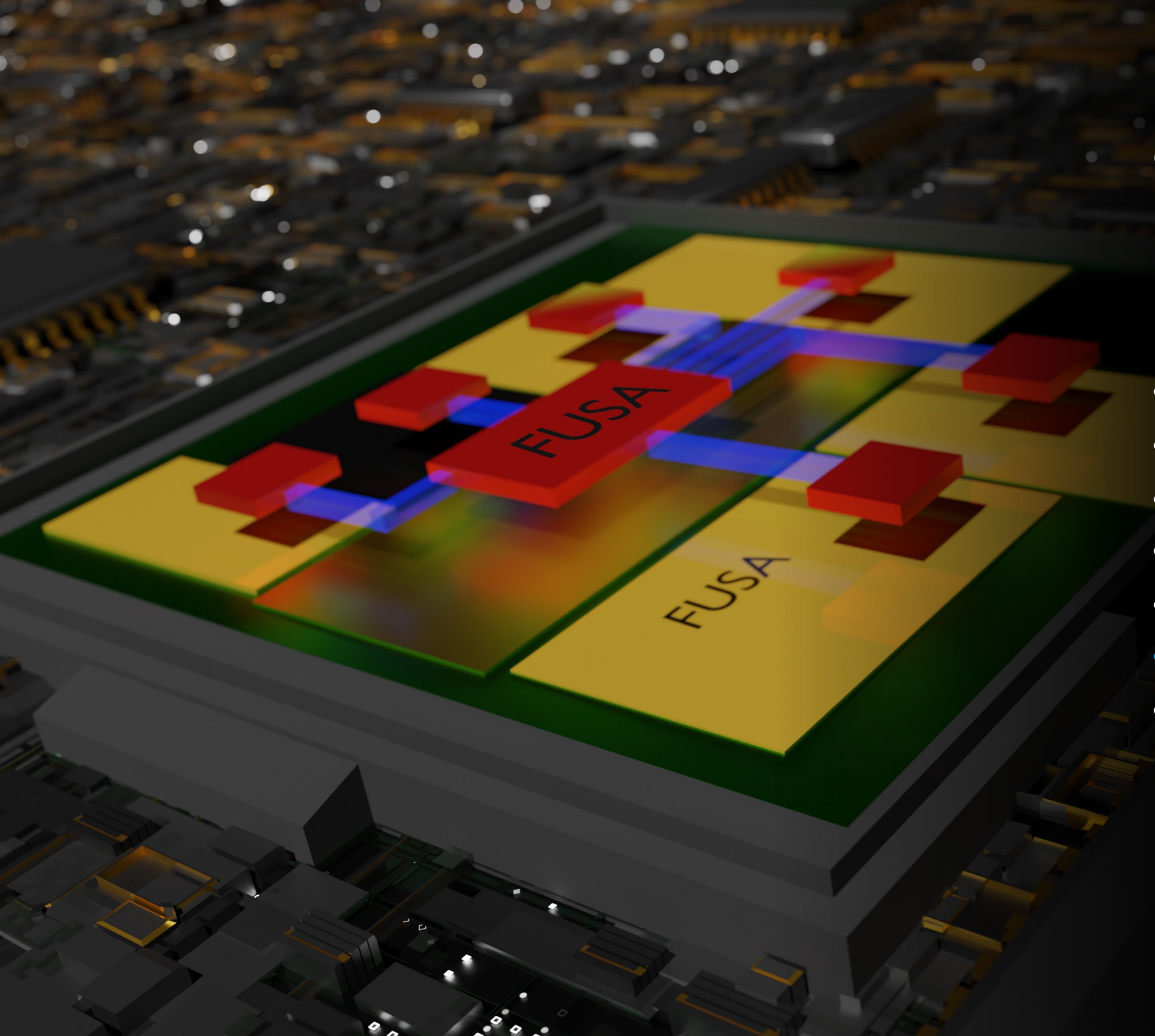
The mSoC* standard

- A market of automotive grade Chiplets
- UCIe™ compliant interconnect
- FUSA Requirement ASIL D / B
- Optimized for Automotive ML workloads
- Secure outliers of ML
- Replacing ”the board” with “the substrate”



*mSoC: Multiple System on Chip

Standardization across chiplets



- Deterministic scheduling of Tasks
- Transport of ASIL D information
- Health/Preventive monitoring
- Diverse Voltage sources for FUSA
- Optimization of workloads from D2D
- ECC uniformity
- Position of I/O and Debugging

Thank you!